

Embargo until September 4, 2006



System-Driven Verification Automation

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TRANSACTION-LEVEL ASSERTIONS ADDED TO JEDA'S NATIVE SYSTEMC ASSERTION TOOLS

Enables System Architects to Write Reusable Checkers at the System-Level

Los Altos, Calif. September 4, 2006—JEDA Technologies today announced the addition of Transaction-Level Assertions (TLA™) capability to its NSCa™ (Native SystemC assertion) family of Native SystemC assertion-based verification automation tools. TLA gives system architects/engineers the ability to create assertion-based checkers at the transaction level.

NSCa, first released in February 2006 supported cycle-level assertions. “What we are doing is addressing the missing capabilities in SystemC by adding temporal expressions and assertions , With TLA, the verification flow from transaction level to cycle level is in place. We see TLA as an effective way to verify system-level models as well as a vehicle to assure system-level requirements are met throughout the design process” said Eugene Zhang, President and CEO of JEDA Technologies.

NSCa is a comprehensive native SystemC assertion development and debug environment for both the transaction-level and cycle-level design phases. NSCa enables a top-down verification process where the architect/systems engineer creates system-level checks that are used throughout the design and verification effort. This executable specification, written as assertions, ensures functional consistency as the design evolves from a system-level description through RTL

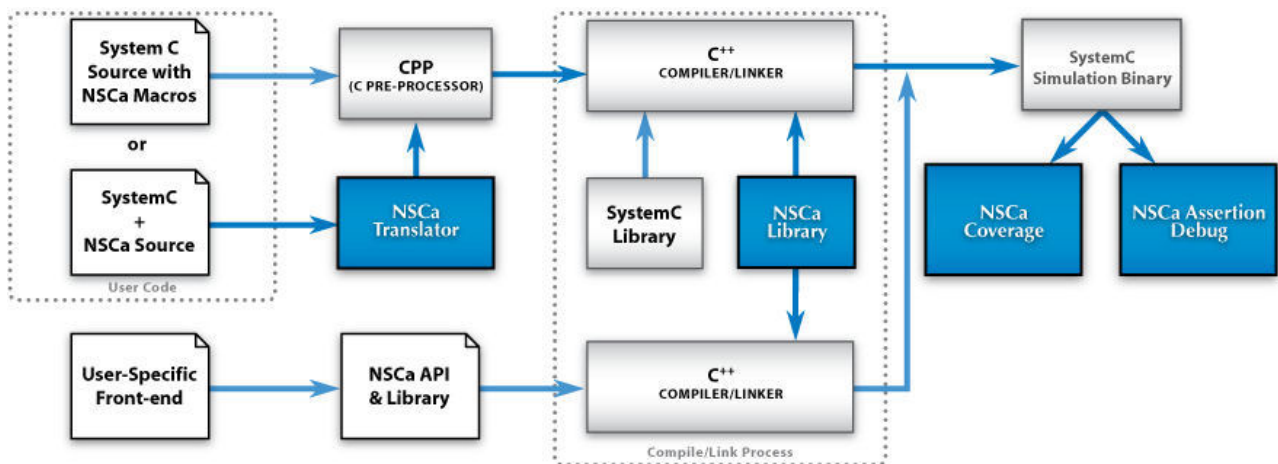
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implementation. These assertions give the verification engineer the ability to reuse and or refine these checks in a testbench environment to quickly find the root cause in a given design problem. Assertion-based testbenches readily pinpoint errors for more efficient debug.

Software developers also benefit from NSCa's use in their virtual prototyping design flow ensures the correctness of their models early in the design phase. During the hardware implementation phase it also helps them validate the consistency between their models and their hardware using the same NSCa codebase.

NSCa easily integrates into an existing SystemC environment. Users have a choice to write their assertion checks in one of three ways:

- 1) Using NSCa assertion macro's which are nothing but C++ macro that can be called directly in any SystemC or C++ functions inside
- 2) Using NSCa extended C++ syntax, a concise and compact assertions syntax that resembles the syntax of SystemVerilog Assertions and or PSL
- 3) Using the language independent API to interface a user-specific front end or C++ codebase



NSCa syntax are few and concise resulting in a 4 to 10x coding efficiency compared to writing assertions directly in SystemC, thus requiring far less code to write and maintain. In addition, NSCa includes a powerful assertion IDE (integrated development environment), an assertion debug environment and assertion coverage and tracing tools. At the cycle-level, the NSCa syntax is very similar to the SVA (SystemVerilog Assertion) syntax or PSL

One of the deficiencies of existing RTL assertion standards is that they do not address the transaction-level. The transaction level is where the systems architect defines the system architecture and specifies the system's performance goals and requirements.

Advanced Assertion Coverage

NSCa includes assertion coverage and advanced assertion path coverage capabilities that record coverage of each possible assertion branch.

Assertion path coverage measures the effectiveness of an assertion description while assertion coverage measures testbench quality.

Experienced Team

The JEDA founding team, Eugene Zhang, CEO; Atsushi Kasuya CTO and Chief Architect; and Teshager Tesfaye, Director of Product Development are the core team that invented Vera at Sun in 1993. Atsushi was the author of all of the original Vera patents. This is the third generation of verification automation tools developed by the JEDA team. The Los Altos team is augmented by a development team in Beijing, China.

About JEDA Technologies

JEDA Technologies, founded in 2002, is the “System-Driven Verification Automation Company” focused on providing automation tools for SystemC based designs. The founding team invented Vera when they were at Sun Microsystems. The company is based in Los Altos, California with an additional development center in Beijing China. For more information, please visit www.jedatechnologies.com.

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